PART NUMBER **CSMRLGXXA**

COMPONENT SPECIFICATION **ISSUE 2**

Component Specification For Hermetically Sealed, Radiation-Hard Latching Solid State Relay

Features	Applications
▪ Low on-state resistance ▪ Selection of Operating Current and Voltage ▪ SPST, SPDT, DPST, DPDT ▪ Full Military temperature range -55°C - +125°C ▪ Military and Space Screening ▪ Compatible with µC Drive ▪ Internally Isolated ▪ Output Currents up to 9A	▪ Designed for $28V_{DC}$ Bus Application ▪ Space Systems/Satellites ▪ Space Battery Management Systems ▪ Bus Control ▪ Aerospace Power Distribution ▪ Power Isolation and Control

DESCRIPTION

ISOCOM Latching Solid State Relays are designed to replace existing electro-mechanical relays (EMR). The CSMRLGXXA is available in the single pole single throw (SPST), single pole double throw (SPDT), double pole single throw (DPST) and double pole double throw (DPDT) configuration. They are resilient to damage from shock and immune to contact-related problems (arcing, contamination) that are associated with mechanical equivalents. They are also lightweight in comparison to the EMR. Coupling between the input, output and power bus stages offers an effective isolation up to 500V. The latch and reset input stages are designed to directly interface with standard microcontrollers (µC), requiring low current (< 10mA) with 3.3V or 5V logic. This device has been designed with an operating voltage of $28V_{DC}$ with current capabilities up to 9A. Furthermore, it is featured in a 12 Pin Flatpack Power Package where each pin is isolated with a glass seal. This package comes with a gold plate finish and solder dip options available.

ISOCOM Limited is AS9100 certified for the design and manufacture of electronic and optoelectronic components.

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STANDARDS

The following specifications have been complied with in the manufacturing of this product –

Aerospace Compliance Standards

AS9100D & ISO 9001:2015 – Design & Manufacture of Electronic and Optoelectronic Components *(Ref GB15/92780)*

Military Compliance Specifications

MIL-PRF-28750 – General Specification for Solid State Relay

Military Compliance Standards

MIL-STD-883 – Test Method Standard Microcircuits

SCREENING INFORMATION

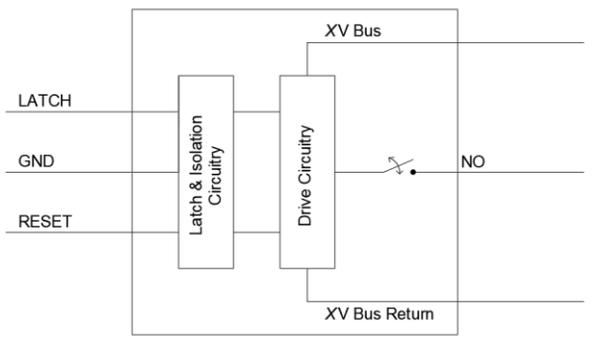
Our LSSR range can be screened to MIL-PRF-28750, applying test methods from MIL-STD-883. Please contact us for more information relating to the applicable screening processes.

FUNCTIONAL DIAGRAMS

*X*V Bus = 28V_{DC}

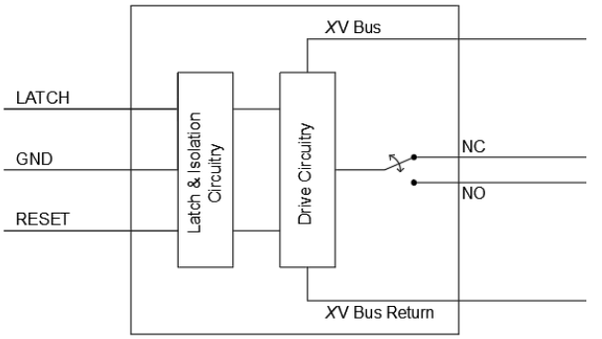
CSMRLGAXA

SPST



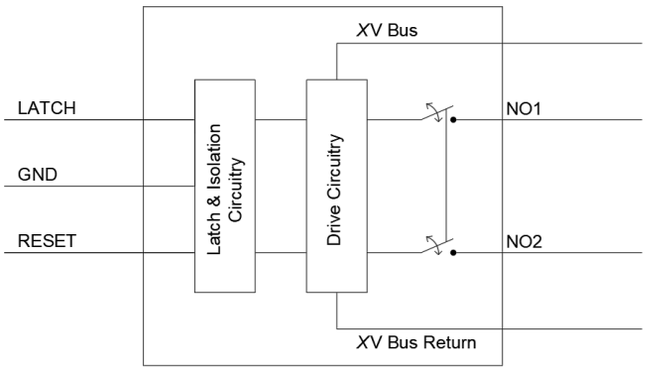
CSMRLGBXA

SPDT



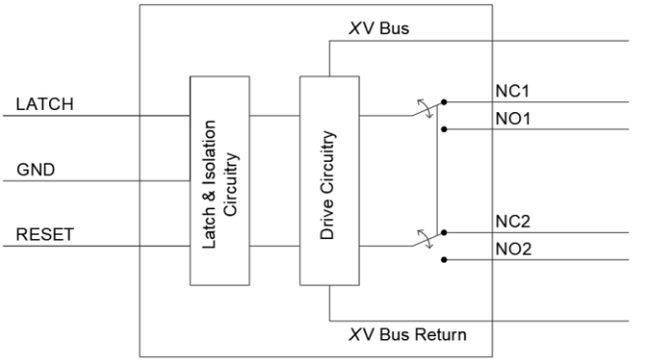
CSMRLGCXA

DPST



CSMRLGDXA

DPDT



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ABSOLUTE MAXIMUM RATINGS

T_A = 25°C U.O.S

Storage Temperature	-65° to +150°C
Operating Temperature	-55° to +125°C
Soldering Temperature	260°C
Continuous Output Current per relay – I_O	See Selection Guide *
Output Voltage- V_O	See Selection Guide +10%
V_{LATCH}	7V
V_{RESET}	7V
I_{LATCH}	15mA
I_{RESET}	15mA
Input-to-Output Isolation Voltage	⇧500 V_{DC}
*X*VBus	28V

*****Current Limited by Package

ELECTRICAL CHARACTERISTICS

T_A= -55°C to +125°C U.O.S

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input						
Latch voltage	V_{Latch}	I_{Latch} = 10mA	3	5	-	V
Reset voltage	V_{Rst}	I_{Rst} = 10mA				
Latch Current	I_{Latch}	V_{Latch} = 5V	7	10	-	mA
Reset Current	I_{Rst}	V_{Rst} = 5V				
Latch/Reset reverse breakdown voltage	$B_{VR(Latch)}$	I_R = 10 µA	5	-	-	V
	$B_{VR(Rst)}$					
Latch pulse duration	PW_{Latch}	V_{Latch} = 5V	40	-	-	µs
Reset pulse duration	PW_{Rst}	V_{Rst} = 5V	40	-	-	µs
Output						
*X*VBus current	$I_{Bus\ (Latched)}$	*X*VBus = 28V, mode = Latch	-	8	-	mA
	$I_{Bus(Unlatched)}$	*X*VBus = 28V, mode = Reset	-	1.5	-	mA
Output current	I_O	*X*VBus = 28V	See selection guide (Page 7)			A
Output on state resistance (per output)	$R_{(On)}$					mΩ
Output leakage Current	I_{OL}		-	10	70	µA
Coupled						
Input-to-output isolation breakdown voltage (1)	V_{I-O}	I_{I-O} in to out = 1µA, T_A = 25°C	-	-	500	V
Latch time (NO Latch) (2)	$T_{PL(NO)}$	*X*VBus = 28V, I_{OX} = See selection guide	-	950	-	µs
Latch time (NC Latch) (2)	$T_{PL(NC)}$		-	150	-	
Reset latch delay (NO to reset) (2)	$T_{PR(NO)}$		-	250	-	
Reset latch delay (NC to reset) (2)	$T_{PR(NC)}$		-	150	-	

Notes:

(1) Inputs shorted together; outputs shorted together

(2) See propagation timing delay measurements

(3) For data on SOA please contact sales at ISOCOM Ltd

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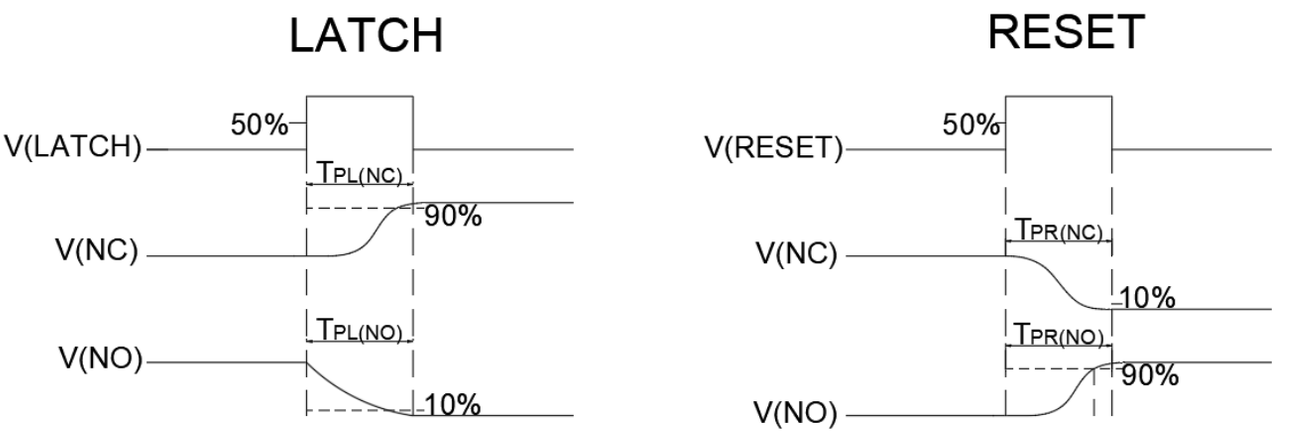
PROPAGATION TIMING DELAY MEASUREMENTS



Switching Characteristics (Note: All Signals Measured with Respect to *X*V Bus Return)

TRUTH TABLE

Bus Voltage	on	on	on	on	on	on	off	on
Latch	0	1	0	0	0	1	X	0
Reset	0	0	0	1	0	0	X	0
NO status	Open	Closed	Closed	Open	Open	Closed	Open	Open
NC status	Closed	Open	Open	Closed	Closed	Open	Open	Closed

On initial powerup the LSSR is in its default condition. The normally open (NO) and normally closed (NC) outputs are open and closed respectively. Upon receiving a short input pulse to the LATCH input, the NO and NC terminals become closed and open circuit respectively. The device will then remain in the latched condition indefinitely or until a short input pulse to the RESET returns the outputs to their default conditions. Additionally, if the 28V bus line is off while the LSSR is in the LATCH state, the device outputs automatically return to their default conditions upon the power reinstatement.

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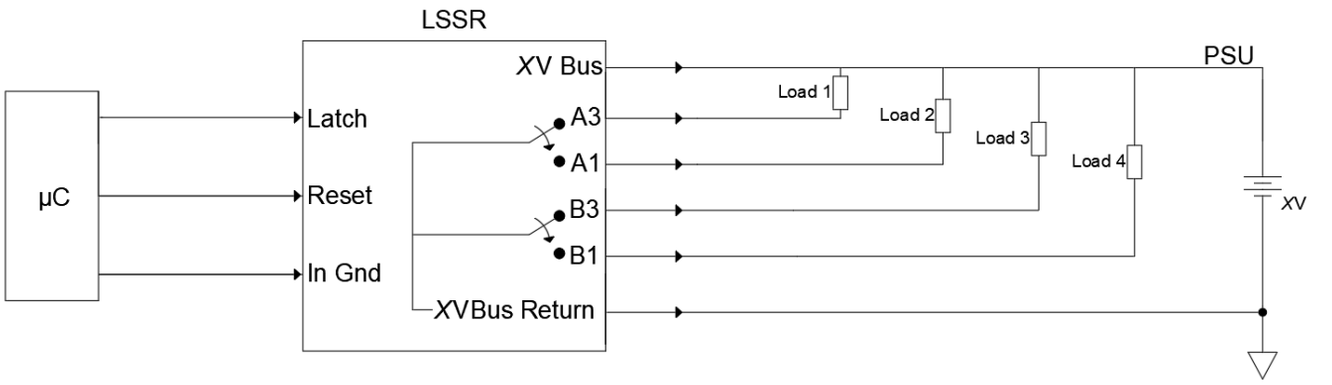
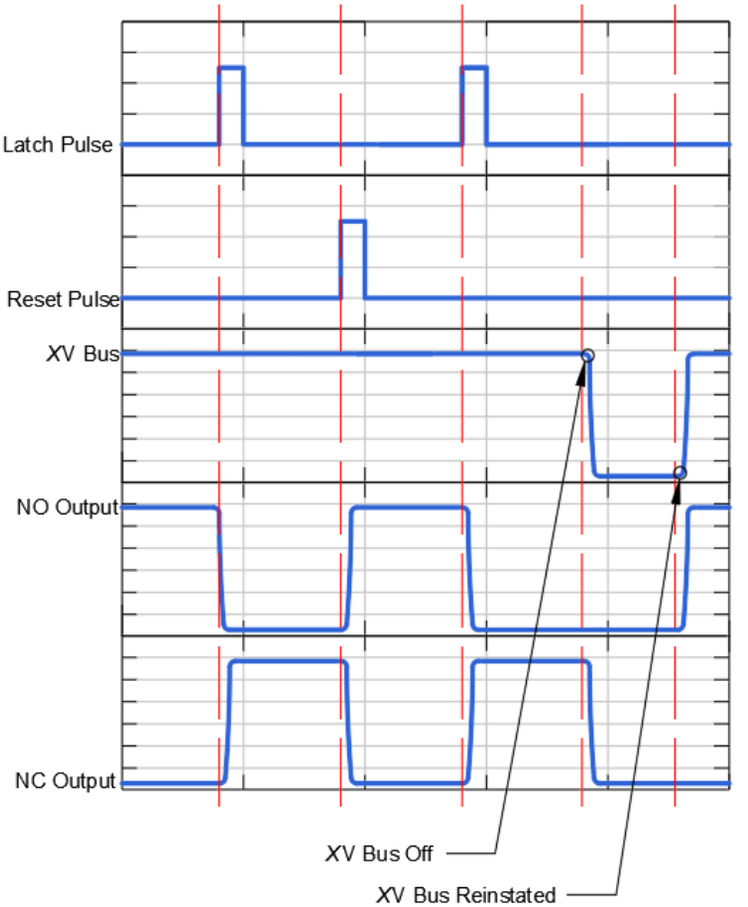
APPLICATIONS

APPLICATION 1



Notes:

- For low side switching
- All loads connected to *X*V
- *X*V Bus Return has the sum of current from all loads and *X*V PSU
- Waveforms below measured at points A1/B1 (NO) and A3/B3 (NC) outputs with respect to *X*VBus Return



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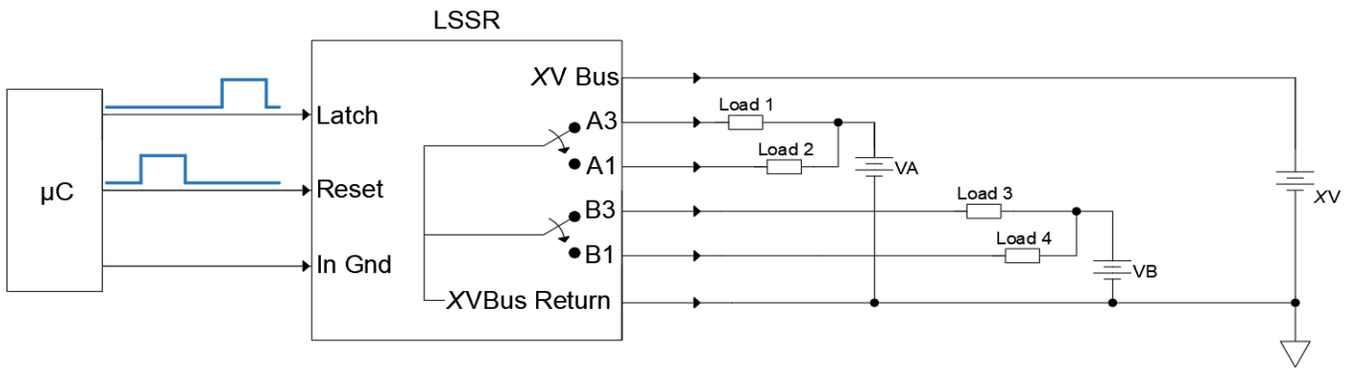
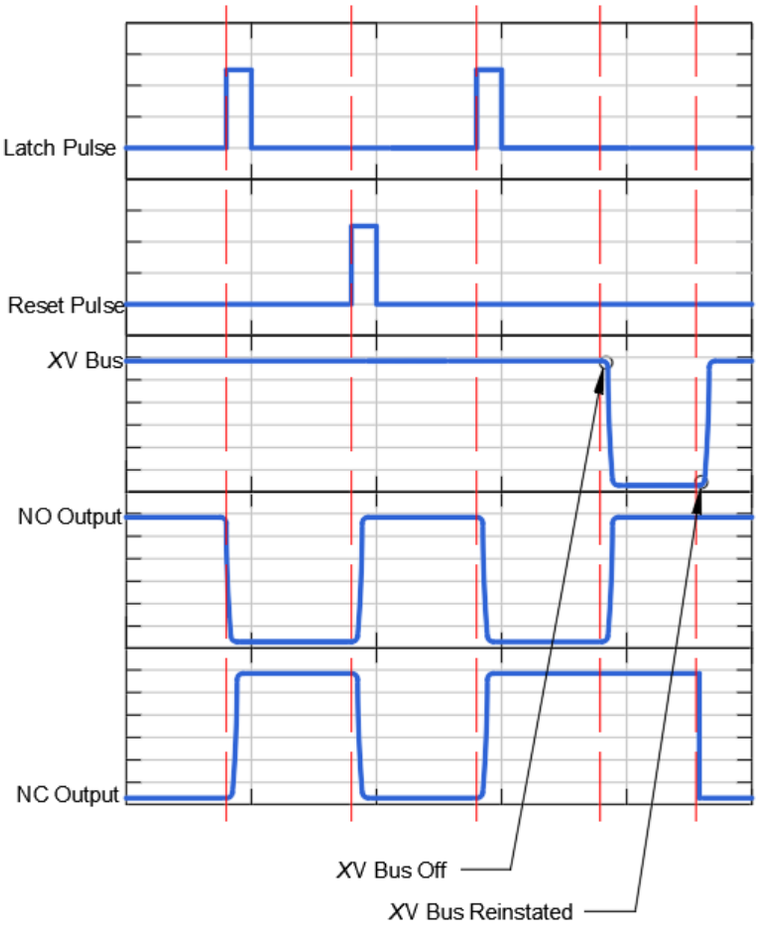
APPLICATION 2



Notes:

- For low side switching
- Can have an *X*V power supply for a virtual V_{CC}
- VA and VB can be independent supplies (and lower than *X*V)
- Can also be expanded to independent PSUs on the loads of A3, A1, B3 and B1
- All output supplies must share the same ground
- *X*V Bus Return has the sum of currents from VA, VB and *X*V
- Waveforms below measured at points A1/B1 (NO) and A3/B3 (NC) outputs with respect to *X*VBus Return



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SELECTION GUIDE

Bus Voltage (V)	I_D (A)	$R_{(ON)}$ (TYP) (mΩ)
28	1 3 5 9	10

ORDERING PARTS

CSMRLG X X A

Part Reference	Circuit	Current (A)	Package Type
CSMRLGXXA	A (SPST) B (SPDT) C (DPST) D (DPDT)	1 3 5 9	Power Package 12 Pin Flatpack

PACKAGE STYLES AND CONFIGURATION OPTIONS

Package	Power Package 12 Pin Flatpack
Lead Style	-
Channels	Optional
Common Channel Wiring	-
ISOCOM Part Number and Options	
Commercial	CSMRLGXXA
Defense Screen Level	CSMRLGXXA/L2
Space Screen Level	CSMRLGXXA/L2S
Standard Gold Plate Finish	Gold Plate
Solder Dipped	Option #20

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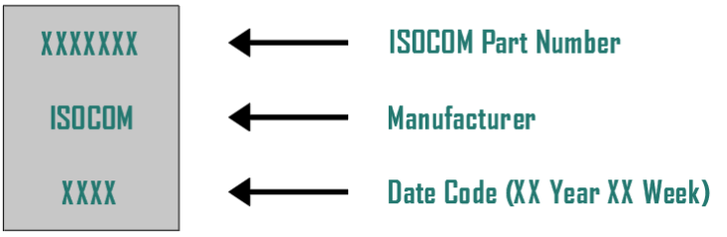
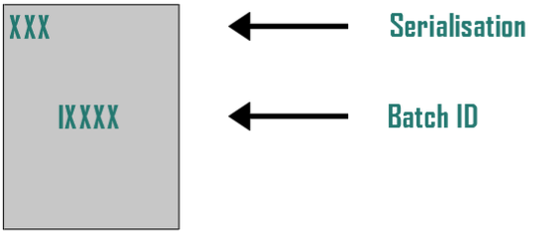
DEVICE MARKING

FRONT OF DEVICE



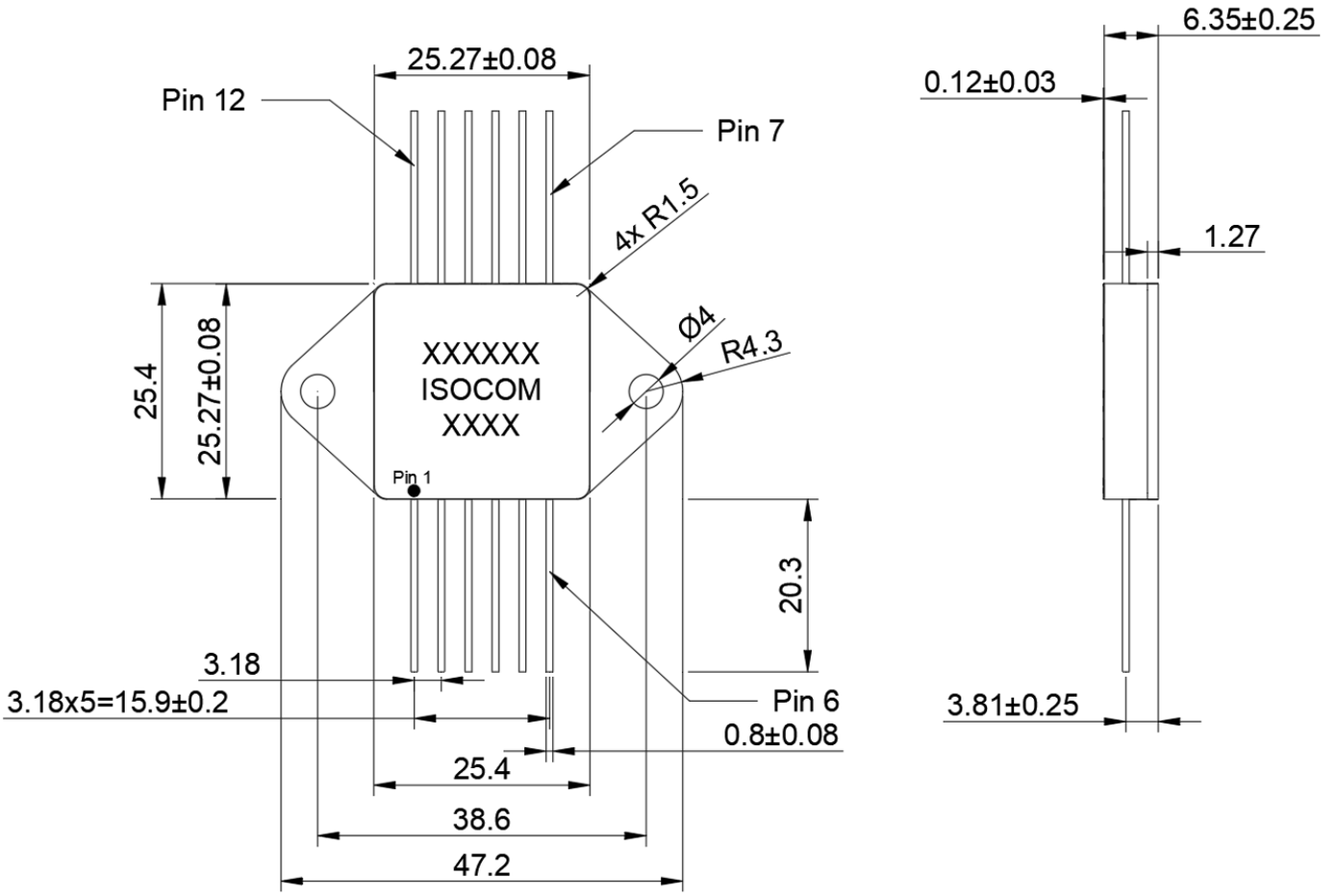
BACK OF DEVICE



FOR SPACE SCREENED PARTS ONLY

OUTLINE DRAWINGS

Power Package 12 Pin Flatpack



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PIN OUT INFORMATION

Pin Number	Pin Function			
	SPST	SPDT	DPST	DPDT
1	*X*VBus	*X*VBus	*X*VBus	*X*VBus
2	Reset	Reset	Reset	Reset
3	GND	GND	GND	GND
4	Latch	Latch	Latch	Latch
5	-	-	NO2	NO2
6	-	-	NO2	NO2
7	-	-	-	NC2
8	-	-	-	NC2
9	NO1	NO1	NO1	NO1
10	NO1	NO1	NO1	NO1
11	-	NC1	-	NC1
12	-	NC1	-	NC1
Case	*X*VBus Return	*X*VBus Return	*X*VBus Return	*X*VBus Return

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