Package, Tape-and-Reel and Pad Layout Specifications

Best-in-Class Miniaturization

Package Drawings

All NVE packages are compliant with JEDEC standards, but some also meet creepage requirements unique to isolators.

**6-pin TDFN**

Dimensions in mm; scale = approx. 10X

**8-pin MSOP**

Dimensions in inches (mm); scale = approx. 5X

NOTE: Pin spacing is a BASIC dimension; tolerances do not accumulate
16-pin QSOP Package

Dimensions in inches (mm); scale = approx. 5X

8-pin SOIC Package

Dimensions in inches (mm); scale = approx. 5X

8-pin PDIP

Dimensions in inches (mm); scale = approx. 2.5X

NOTE: Pin spacing is a BASIC dimension; tolerances do not accumulate
0.15" 16-pin SOIC Package (-3 suffix)

Dimensions in inches (mm); scale = approx. 5X

Pin 1 identified by either an indent or a marked dot

0.007 (0.2)
0.013 (0.3)

0.013 (0.3)
0.020 (0.5)

0.055 (1.40)
0.062 (1.58)

0.054 (1.4)
0.072 (1.8)

0.016 (0.4)
0.050 (1.3)

NOTE: Pin spacing is a BASIC dimension; tolerances do not accumulate

NOM

Dimensions in inches (mm); scale = approx. 5X

Pin 1 identified by either an indent or a marked dot

0.007 (0.2)
0.013 (0.3)

0.013 (0.3)
0.020 (0.5)

0.055 (1.40)
0.062 (1.58)

0.054 (1.4)
0.072 (1.8)

0.016 (0.4)
0.050 (1.3)

NOTE: Pin spacing is a BASIC dimension; tolerances do not accumulate

*Specified for True 8™ package to guarantee 8 mm creepage per IEC 60601.
Tape-and-Reel Specifications

Tape-and-Reel Dimensions

<table>
<thead>
<tr>
<th>Tape Width</th>
<th>( D_0 )</th>
<th>( E_1 )</th>
<th>( F )</th>
<th>( P_0 )</th>
<th>( P_1 )</th>
<th>( P_2 )</th>
<th>( W )</th>
<th>( T )</th>
</tr>
</thead>
<tbody>
<tr>
<td>8 mm</td>
<td>1.5±0.10</td>
<td>1.75±0.10</td>
<td>3.5±0.05</td>
<td>4.0±0.10</td>
<td>2.0±0.05</td>
<td>8.0±0.30</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12 mm</td>
<td></td>
<td></td>
<td>5.5±0.05</td>
<td>8.0±0.10</td>
<td>12.0±0.30</td>
<td>0.40 Max</td>
<td></td>
<td></td>
</tr>
<tr>
<td>16 mm (narrow SOIC)</td>
<td></td>
<td></td>
<td>7.5±0.10</td>
<td>8.0±0.10</td>
<td>2.0±0.10</td>
<td>16.0±0.30</td>
<td></td>
<td></td>
</tr>
<tr>
<td>16 mm (wide SOIC)</td>
<td></td>
<td></td>
<td>12.0±0.10</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Dimensions in millimeters

Tape-and-Reel Part Orientation

<table>
<thead>
<tr>
<th>Package</th>
<th>Carrier Tape Width</th>
<th>Standard Quantities</th>
<th>Width x Pitch</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5 x 2.5 mm TDFN</td>
<td>8 mm</td>
<td>Qty on 7” Reel 2500</td>
<td>8 x 4 mm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Qty on 13” Reel 5000</td>
<td></td>
</tr>
<tr>
<td>3 x 3 mm TDFN</td>
<td>12 mm</td>
<td></td>
<td>12 x 8 mm</td>
</tr>
<tr>
<td>MSOP</td>
<td>12 mm</td>
<td>Qty on 7” Reel 1000</td>
<td>12 x 8 mm</td>
</tr>
<tr>
<td>SOIC 8</td>
<td>12 mm</td>
<td>Qty on 7” Reel 1000</td>
<td>12 x 8 mm</td>
</tr>
<tr>
<td>SOIC 16 Narrow</td>
<td>16 mm</td>
<td>Qty on 7” Reel 800</td>
<td>16 x 8 mm</td>
</tr>
<tr>
<td>SOIC 16 Wide</td>
<td>16 mm</td>
<td>Qty on 13” Reel 3000</td>
<td>16 x 12 mm</td>
</tr>
<tr>
<td>1.1 x 1.1 mm ULLGA</td>
<td>8 mm</td>
<td>Qty on 7” Reel 2500</td>
<td>8 x 4 mm</td>
</tr>
<tr>
<td>4.9 x 6.0 mm TDFN</td>
<td>12 mm</td>
<td>Qty on 13” Reel 5000</td>
<td>12 x 8 mm</td>
</tr>
</tbody>
</table>
### Recommended Pad Layouts

NVE recommends pad layouts with wider pad spacing than most libraries to avoid compromising isolator creepage and clearance:

#### 6-pad TDFN Pad Layout

Dimensions in inches (mm); scale = approx. 5X

<table>
<thead>
<tr>
<th>Width</th>
<th>Height</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.133 (3.38)</td>
<td>0.065 (1.65)</td>
</tr>
<tr>
<td>0.026 (0.65)</td>
<td>0.012 (0.30)</td>
</tr>
</tbody>
</table>

6 PLCS

#### 8-pin MSOP Pad Layout

Dimensions in inches (mm); scale = approx. 5X

<table>
<thead>
<tr>
<th>Width</th>
<th>Height</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.227 (5.77)</td>
<td>0.120 (3.05)</td>
</tr>
<tr>
<td>0.025 (0.65)</td>
<td>0.017 (0.43)</td>
</tr>
</tbody>
</table>

8 PLCS

#### 8-pin QSOP Pad Layout

Dimensions in inches (mm); scale = approx. 5X

<table>
<thead>
<tr>
<th>Width</th>
<th>Height</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.275 (6.99)</td>
<td>0.160 (4.05)</td>
</tr>
<tr>
<td>0.025 (0.635)</td>
<td>0.012 (0.30)</td>
</tr>
</tbody>
</table>

16 PLCS
8-pin SOIC Pad Layout

Dimensions in inches (mm); scale = approx. 5X

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Value (inches)</th>
<th>Value (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Height</td>
<td>0.275</td>
<td>6.99</td>
</tr>
<tr>
<td>Width</td>
<td>0.160</td>
<td>4.05</td>
</tr>
<tr>
<td>Lead Length</td>
<td>0.050</td>
<td>1.27</td>
</tr>
<tr>
<td>Placing</td>
<td>0.020</td>
<td>0.51</td>
</tr>
<tr>
<td>Package Size</td>
<td>8 PLCS</td>
<td></td>
</tr>
</tbody>
</table>

0.15" 16-pin SOIC Pad Layout

Dimensions in inches (mm); scale = approx. 5X

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Value (inches)</th>
<th>Value (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Height</td>
<td>0.275</td>
<td>6.99</td>
</tr>
<tr>
<td>Width</td>
<td>0.160</td>
<td>4.05</td>
</tr>
<tr>
<td>Lead Length</td>
<td>0.050</td>
<td>1.27</td>
</tr>
<tr>
<td>Placing</td>
<td>0.020</td>
<td>0.51</td>
</tr>
<tr>
<td>Package Size</td>
<td>16 PLCS</td>
<td></td>
</tr>
</tbody>
</table>
### 0.3" 16-pin SOIC Pad Layout

Dimensions in inches (mm); scale = approx. 5X

- **0.317 (8.05)**
- **0.050 (1.27)**
- **0.020 (0.51)**
- **0.449 (11.40)**

16 PLCS
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